

a substrate having an exposed region of a silicon-containing semiconductor material; and

a first layer of metal disilicide having lateral edges, wherein said metal of said disilicide is selected from the group consisting of Ti, Co and mixtures thereof, and said exposed region of said substrate and said first layer are separated by a Si-Ge interlayer, said Si-Ge interlayer having lateral edges which do not substantially extend beyond the lateral edges of the metal disilicide...-

**REMARKS**

Favorable reconsideration and allowance of the claims of the present application are respectfully requested.

In the present Office Action, the Examiner alleges that applicants' previous Amendments dated January 6, 2003 and October 22, 2002 were not fully responsive since a marked-up version of the claims was allegedly not submitted which included underlining of all the additions made to Claim 23.

In light of the above, applicants provide herewith a clean copy as well as a marked-up copy of the amendments that were intended to be made in the Response dated October 22, 2002. The marked-up version is included within the attachment captioned as "**MARKED-UP VERSION SHOWING CHANGES MADE**".

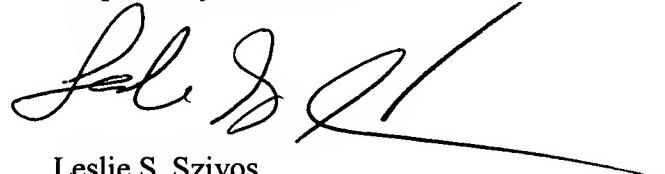
Applicants respectfully submit the amendments made herein are in compliance with existing U.S. Patent and Trademark guidelines since the same includes underlining of all material inserted into Claim 23.

Applicants respectfully submit that the remarks provided at Pages 2-6 of the previous Response dated October 22, 2002, including the remarks where support for the amendments to the claims are provided, are incorporated herein by reference.

Applicants respectfully submit that this Response, together with the previous Response dated October 22, 2002, are fully responsive to the Office Action dated July 22, 2002.

Wherefore, reconsideration and allowance of the claims of the present application are respectfully requested.

Respectfully submitted,



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**VERSION WITH MARKINGS SHOWING CHANGES MADE IN THE CLAIMS:**

Please cancel Claims 29 and 30, without prejudice or disclaimer, and please amend Claim 23 to read as follows:

23. (Amended) An electrical contact to a region of a silicon-containing substrate comprising:

a substrate having an exposed region of a silicon-containing semiconductor material; and

a first layer of metal disilicide which includes an additive or Ge, wherein said metal of said disilicide is selected from the group consisting of Ti, Co and mixtures thereof, and said exposed region of said substrate and said first layer are separated by a Si-Ge interlayer.

**Please add the following new claims:**

--36. The electrical contact of Claim 23 wherein said additive is selected from the group consisting of C, Al, Si, Sc, Ti, V, Cr, Mn, Fe, Co, Ni, Cu, Y, Zr, Nb, Mo, Ru, Rh, Pd, In, Sn, La, Hf, Ta, W, Re, Ir, Pt, Ce, Pr, Nd, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb, Lu and mixtures thereof.

37. The electrical contact of Claim 36 wherein said additive is C, Al, Si, Sc, Ti, V, Cr, Mn, Fe, Co, Ni, Cu, Y, Zr, Nb, Mo, Ru, Rh, Pd, In, Sn, La, Hf, Ta, W, Re, Ir, Pt or mixtures thereof

38. The electrical contact of Claim 37 wherein said additive is Si, Ti, V, Cr, Ni, Nb, Rh, Ta, Re, Ir or mixtures thereof.

39. The electrical contact of Claim 23 wherein said additive is present in said metal disilicide in an amount of from about 0.01 to about 50 atomic percent.

40. An electrical contact to a region of a silicon-containing substrate comprising:

a substrate having an exposed region of a silicon-containing semiconductor material;

and

a first layer of metal disilicide having lateral edges, wherein said metal of said disilicide is selected from the group consisting of Ti, Co and mixtures thereof, and said exposed region of said substrate and said first layer are separated by a Si-Ge interlayer, said Si-Ge interlayer having lateral edges which do not substantially extend beyond the lateral edges of the metal disilicide.--